CLAIMS

1. (Currently amended) A semiconductor device having operation modes of a first mode and a second mode with reduced current consumption relative to that of the first mode, comprising:

a main power supply line;

a sub power supply line;

a first switch circuit connecting said sub power supply line to said main power supply line in said first mode and disconnecting said sub power supply line from said main power supply line in said second mode; and

an internal circuit operating according to an input signal in said first mode and entering a standby state in said second mode,

said internal circuit including

a first field-effect transistor having a gate insulating film with a predetermined thickness and kept in a non-conductive state in said second mode;

a second field-effect transistor connected to said main power supply line, having a gate insulating film with a thickness greater than said predetermined thickness and kept in a conductive state in said second mode; and wherein

said first mode is a normal mode,

said second mode is a power down mode,

said semiconductor device further has an operation mode of a deep power down mode with current consumption reduced relative to that of said power down mode, and

said semiconductor device further comprises a second switch circuit provided between said main power supply line and a power supply node and disconnecting said power supply node from said main power supply line in said deep power down mode.

Claim 2. (Cancelled).

3. (Original) A semiconductor device having operation modes of a first mode and a second mode with reduced current consumption relative to that of the first mode, comprising:

a first internal circuit provided with a power supply potential in said first and second modes;

a second internal circuit activated in said first mode and including at least one field-effect transistor of a first type;

a transmission gate connecting an output of said second internal circuit to an input node of said first internal circuit in said first mode and disconnecting said output from said input node in said second mode, and including a field-effect transistor of a second type having a gate insulating film thicker than that of said field-effect transistor of the first type; and

a third internal circuit including at least one said field-effect transistor of the second type, activated in said second mode and driving said input node.

4. (Original) The semiconductor device according to claim 3, wherein

said first internal circuit is a level conversion circuit converting an amplitude of an input signal corresponding to a first power supply potential into an amplitude corresponding to a second power supply potential to output the resultant amplitude, and

said third internal circuit is a clocked inverter activated in said second mode and inactivated in said first mode.

5. (Currently amended) A semiconductor device having operation modes of a self-refresh mode and a normal mode comprising:

a memory array of dynamic type;

a first internal circuit including at least one field-effect transistor of a first type, activated in said normal mode and inactivated in said self-refresh mode; [[and]]

a second internal circuit including at least one field-effect transistor of a second type having a gate insulating film thicker than that of said field-effect transistor of the first type and activated in said self-refresh mode; and further having an operation mode of a deep power down mode and further comprising a switch for cutting off a power supply current to said second internal circuit in said deep power down mode.

Claim 6. (Cancelled).

7. (Currently amended) A semiconductor device comprising:

a signal line precharged to a first potential in a standby state;

a first field-effect transistor coupling said signal line to a second potential different from said first potential; [[and]]

a second field-effect transistor coupling said signal line to said first potential in said standby state and having a gate insulating film thicker than that of said first field-effect transistor, and further comprising a memory array, wherein

said signal line is a data line for communication of storage data between said memory array and any external element.

Claim 8. (Cancelled).